A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors

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Abstract—**A new CMOS integrated circuit measures the time interval between two digital voltage pulses and stores the result as an analog voltage. Resolution of the circuit is in the subnanosecond range. An additional feature of the circuit is a storage depth of eight samples, i.e., eight consecutive time measurements may be recorded individually and saved in an analog memory.**

I. Introduction

A time-to-voltage converter (TVC) has been designed which measures time intervals over a linear range of 6.5 to 27 ns with an accuracy of 0.3 ns. The range is adjustable to longer intervals with a corresponding loss in accuracy. The measurement is stored as an analog voltage on a capacitor. An additional feature of the circuit is the implementation of an analog memory which allows a series of time-to-voltage conversions to be performed in rapid succession. Close matching between the memory channels allows a total accuracy of 0.4 ns. This circuit has direct applications to instrumentation for high-energy physics experiments (e..g, the Fermilab Tevatron or the Superconducting Super Collider) [1], [2]. It also could be used in phase-locked loops, laser remote sensing (lidar), and time-of-flight detectors (medical tomography).

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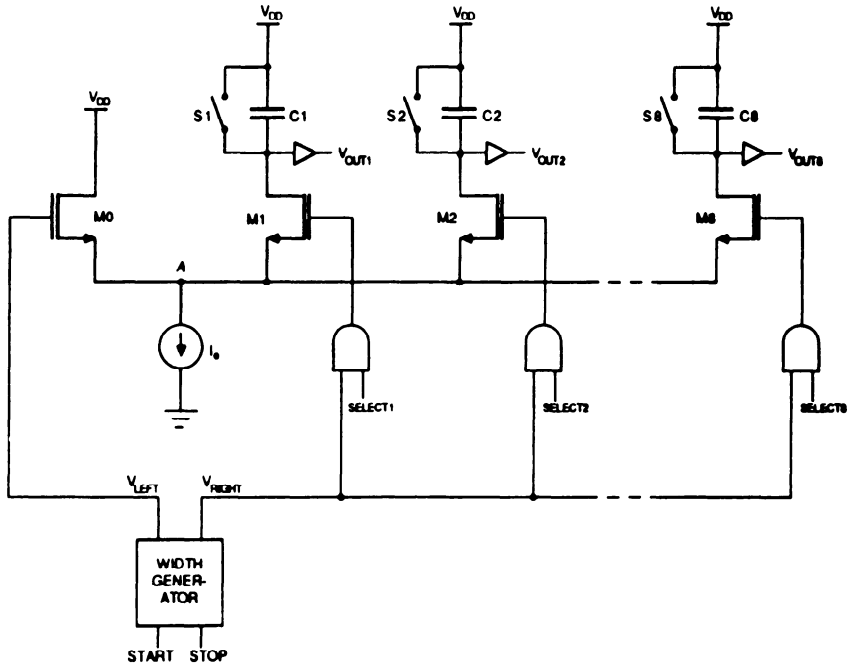

Fig. 1. Schematic of the TVC and analog memory.

The monolithic TVC/analog memory circuit contains eight memory channels and has a total area of 2300 mil^2.

II. Basic Design Considerations

A schematic diagram of the system configuration is shown in Fig. 1. The circuit inputs are the digital *START* and *STOP* signals which mark the beginning and end of the time interval to be measured. These signals are fed to a width generator that generates a digital pulse which is ON for the duration of the time interval. Eight other digital signals (*SELECT* 1–*SELECT* 8) are used to enable one of the eight storage capacitors ($C1$–$C8$) via the AND gates. The complementary outputs of the width generator are then used to steer the current I_o from $M0$ to Mn and then back to $M0$. The resulting voltage on the capacitor will be proportional to the time of charging, and will obey the equation

$$V_C = \frac{I_o}{C} t \tag{1}$$

where t is the time interval being measured and $C = C1 = C2 = \cdots = C8$. Once a capacitor has been charged, the next capacitor is set up to receive the next measurement.

A. Time-to-Voltage Converter

A detailed circuit for the analog section of a single-channel TVC is shown in Fig. 2. An n-channel transistor is used as the storage capacitor. Because this capacitor is always biased heavily in the inversion region, it will provide a highly voltage-independent characteristic. Initially, the switch $S1$ is closed and opened to precharge the capacitor to V_{DD}. After a measurement, the resulting output voltage can be read nondestructively via an appropriate output buffer. Nominal values for I_o and $C1$ are 50 μA and 1 pF, respectively.

The voltages at the gate of $M0$ and $M1$ are digital signals which switch differentially between ground and V_{DD}. It is important to note that the two transistors $M0$ and $M1$ do *not* operate as MOS analog switches in the linear region. Instead, these transistors operate in the saturated region, and the circuit functions similar to a differential pair. If $M0$ and $M1$ were operated as pass transistors, then an uncertainty would exist at the instant of switching: first, if both transistors were off momentarily, the current source would be connected to a floating node, resulting in a large change in the node voltage; alternately, if both transistors were on momentarily, a sneak path would exist between the capacitor and V_{DD}, thus bleeding charge off of the capacitor. By operating in the saturated region, the first problem still exists, but the second problem is eliminated due to the inherent current-flow characteristics of the saturated transistor. Since the drain current in saturation can only flow in one direction (unlike the linear transistor, where the current direction depends on the drain–source voltage), no short-circuit condition will exist. Thus, at the beginning of the measurement, the following chain of events takes place in rapid succession: a) initially, $M0$ is ON, $M1$ is OFF, and no current flows to the capacitor; b) then, after the *START* signal is received, $M1$ is turned ON *before* $M0$ is turned OFF, and the two transistors supply current for a short time; c) finally, $M0$ is turned OFF completely, and all of the current flows through $M1$. Discharging of the storage capacitor then takes

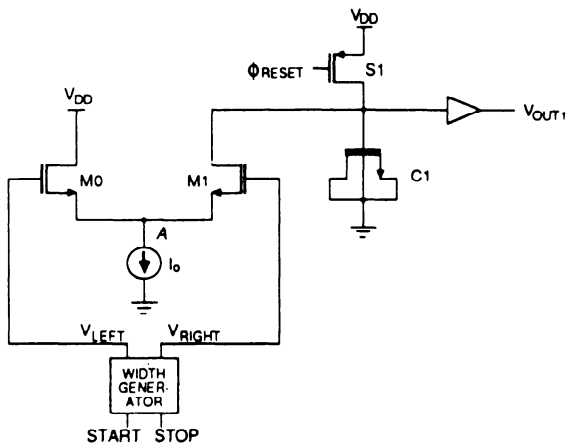

Fig. 2. Single-channel TVC.

place, and at the end of the measurement, the procedure is reversed. The resulting capacitor voltage will contain two components: a linear portion which is proportional to the time interval, and an offset which will depend on the length of the time that both transistors are ON. However, as long as a stable set of overlapping gate pulses can be generated for $M0$ and $M1$ by the width generator, the offset will be constant and reproducible.

The measurement range of the circuit is limited by two different effects. The minimum measurable time will be determined by the smallest time difference between *START* and *STOP* that can be resolved by the width generator, which is about 5 ns. The maximum time is limited by the operating point of $M1$; as the capacitor is discharged, V_{DS1} will decrease, eventually sending $M1$ out of saturation and into the linear region. This effect constrains the maximum voltage swing on the capacitor to the threshold voltage V_{T1}, corresponding to a maximum measurement time of about 25 ns. It should be noted that the maximum measurement interval could be arbitrarily increased or decreased by adjusting I_o, which would cause an inverse change in time resolution as well. Alternatively, the measurement range could be increased by initially charging the storage capacitor to a higher voltage (instead of directly to V_{DD}); however, this would require an added external reference voltage.

Several parasitic elements are important in the design of the TVC. The capacitance at the sources of the transistors is most significant. This capacitance (cumulatively referred to as C_P) consists of the source—bulk junctions of $M0$ and $M1$, the drain–bulk junction of the current source, and the interconnection wire between these three circuit elements. Other important parasitics include the gate–source and gate–drain overlap capacitances and the channel charge. The effect of parasitic capacitances on circuit operation is displayed in Fig. 3. This SPICE simulation [3] assumes ideal voltage generators (V_{LEFT} and V_{RIGHT}) as the drive for the gates of $M0$ and $M1$ and an ideal current source for I_o. The resulting drain current (I_{D1}) shows the feedthrough effects during switching of the overlap capacitances c_{gd1}, c_{gs1}, and c_{gs0}. The feedthroughs appear as constant currents because V_{LEFT} and V_{RIGHT} are modeled as ideal sources; in reality, the feedthroughs will be current spikes. These feedthrough currents of about 10 μA will be on the same order as I_o and are not negligible. However, the feedthrough at turn-on will be of the same magnitude but of the opposite direction as the feedthrough at turn-off, making the net effect nearly zero. In order to overcome the effect of the channel charge, small-geometry devices are used to reduce the effect to an unobservable level.

The simulation also shows the effect of C_p on the switching mechanism. A large C_P will slow down the circuit by limiting the slew rate at the source node (hereafter referred to as node A). This in turn will cause the transient effects due to switching to take longer to die out. Thus, the size of C_P must be minimized because it will affect the linearity of the time measurement for small intervals due to the nonlinear charging of the storage capacitor during the transient. This minimization is accomplished by carefully controlling the transistor source areas and interconnect area at node A.

B. Analog Memory

The eight-channel analog memory is easily implemented by adding more transistor–capacitor combinations on the right side of the single-channel version (Fig. 1). Thus, an arbitrary number of TVC's can be integrated into a single system, limited by the added parasitic capacitance at node A. An 8-bit shift register is used to select among the channels (not shown).

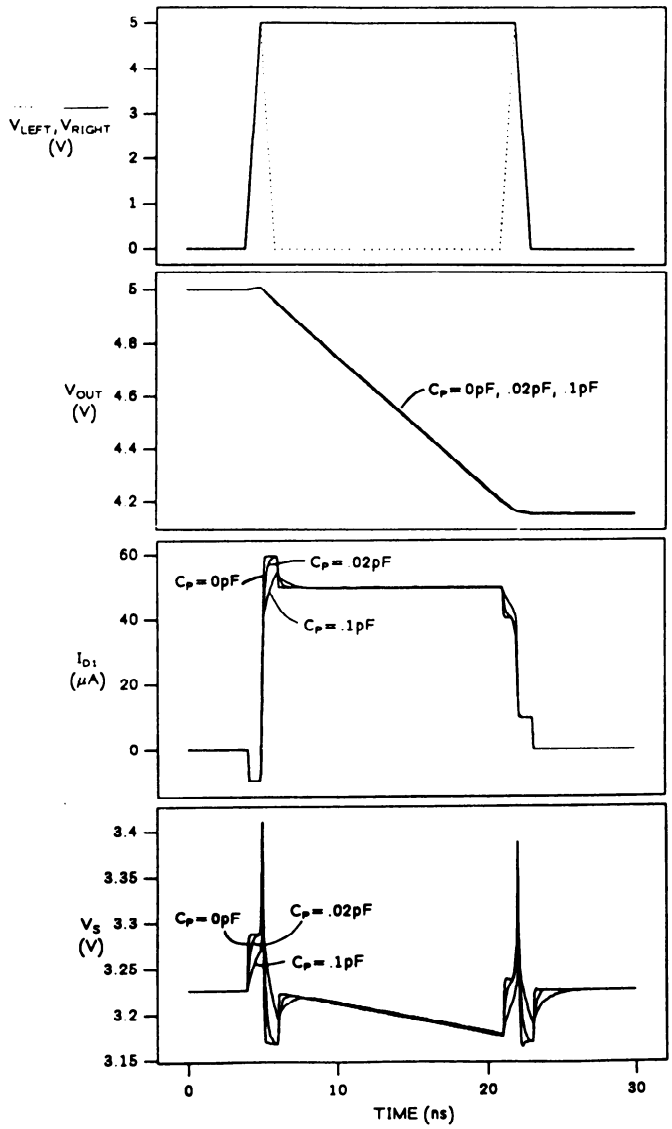

Fig. 3. SPICE simulation of the TVC.

The matching of components between channels is important in order to maintain a constant level of performance across the system. However, it is more critical for certain components to be matched than others. In particular, the hold capacitors must be matched as closely as possible because variations in the absolute value of the capacitor will have a first-order effect on the output voltage. Capacitor matching is accomplished through use of various layout techniques, including common-centroid geometry. Matching of the other channel components is less critical because the effects will be second order. In the case of the switching transistors, process variations will cause changes in W, L, and V_T. However, since the transistor current is always set by I_o, the variations will cause a change in V_{GS}; this will in turn cause a fluctuation on V_S, but will not affect accuracy. Threshold variations can also affect the logic at the gates of the switching transistors. These variations can cause a shift in the logic threshold level of the gate, corresponding to an uncertainty of the precise instant when the gate will switch from high to low. In order to reduce this uncertainty, the logic which drives the current switch is always overdriven so that the rise times will be as short as possible. This reduces any logic skew to a minimum.

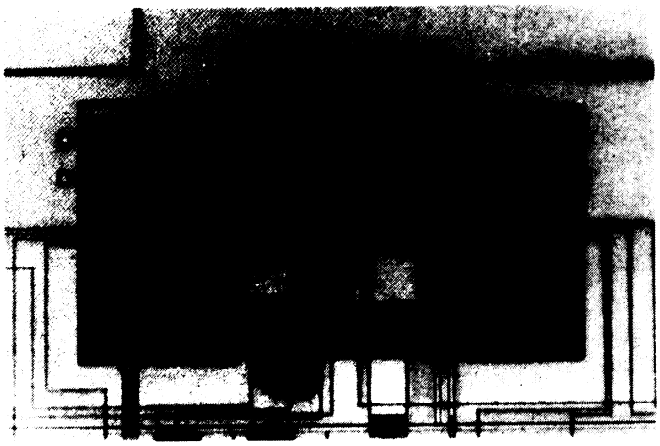

Fig. 4. Photomicrograph of the TVC/analog memory circuit. Size: 2300 mil^2.

TABLE I
TVC/ANALOG MEMORY PERFORMANCE

Linear Measurement Range	6.5–27 ns
Output Swing	1.06 V
Single Channel:	
Noise (jitter)	± 3.5 mV
Integral Non-linearity	± 7.0 mV
Total Accuracy[1]	± 8.0 mV (± 0.15 ns resolution)
8-Channels:	
Error due to mismatch	± 7.5 mV
Total Accuracy[2]	± 11.0 mV (± 0.2 ns resolution)
Power Dissipation:	
not including output buffers	2 mW
including 8 output buffers	45 mW
Power Supply Rejection Ratio	15 dB
Temperature Dependence	750 ppm/°C (10 ps/°C)

[1]Single channel accuracy is noise and non-linearity added in quadrature.
[2]8-channel accuracy is noise, non-linearity, and mismatch added in quadrature.

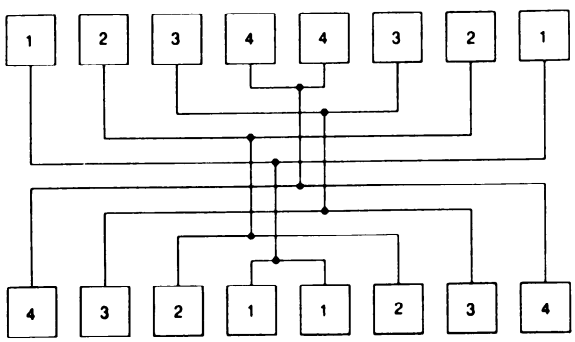

Fig. 5. Common-centroid layout of the storage capacitors.

TABLE II
TVC/ANALOG MEMORY CHIP-TO-CHIP VARIATION

	$\bar{x}$	σ_x	$\frac{\sigma_x}{\bar{x}}$ (%)
Current Source	49.08 μA	0.354 μA	0.72
Storage Capacitor	0.888 pF†	0.00615 pF†	0.69
Output Buffer Gain	0.929	0.00340	0.37
TVC Transfer Ratio	51.32 mV/ns	0.913 mV/ns	1.78

†derived

III. LAYOUT

Eight channels of analog memory were implemented on the prototype chip (Fig. 4). The number eight is a compromise between depth of memory and two constraints. First, as previously mentioned, for a good transient response and settling time, the capacitance at node *A* had to be minimized. The second constraint was layout complexity; due to the stringent matching requirement on the capacitors, most of the circuitry for the eight channels had to be laid out in one piece—it was not possible to design one channel and then repeat it any number of times. Thus, a total of eight channels provided a good measure of circuit performance while also keeping the layout tractable and the node *A* capacitance reasonable.

In order to best match the eight channels, each capacitor was split into four identical smaller components which were located around a common centroid. An example of this scheme is shown in Fig. 5, where four channels have been laid out. A key feature of this particular method is that the total area of the interconnection wiring will be identical for each channel; although the wiring will not be common centroid, it will be matched as closely as possible. This becomes important as more capacitors are added to the array and the interconnect capacitance adds a nonnegligible component to the total hold capacitance.

IV. TEST RESULTS

A summary of the circuit performance is shown in Table I. Linearity of the TVC was measured to be highly accurate over an input range of 6.5 to 27 ns. Deviations in circuit performance were due to three effects: random noise, nonlinearity, and mismatch. The main source of noise was the external environment via the power supply. Noise performance was optimized by using a V_{DD} and V_{SS} of 0 and -5 V, respectively, which limited the noise effect to fluctuations on the 50-μA current source. This resulted in a ± 3.5-mV jitter on all time measurements. Integral nonlinearity was measured by finding the worst-case deviation from a best-fit line on the transfer characteristic. Among the eight channels, the worst nonlinearity on any channel was ± 7.0 mV. This was caused by nonlinearities in the MOS hold capacitor, parasitic junction capacitances, and variation in the current source due to voltage changes at node *A*. Variation of the transfer characteristic slopes of the eight TVC channels was caused by mismatch on the capacitors, thresholds, and output buffers. These factors caused a worst-case error of ± 7.5 mV. However, it is assumed that much of the mismatch was due to gain variation on the eight output buffers (source followers), and that a multiplexed readout system would greatly enhance performance.

Power dissipation in the actual TVC circuit is low, consisting of a static 50-μA current plus some digital logic. The bulk of the power is in the output buffers, which could be reduced by a multiplexed readout. A statistical analysis of the circuit performance from chip to chip is shown in Table II. This table shows the mean and standard deviation for several circuit parameters, including the current source magnitude, the output buffer gain, and the TVC transfer ratio. In addition, the statistics for the storage capacitor were computed via (1) (the capacitors were not directly measurable in the lab). Thus, although the nominal value of the capacitor was off as expected (by 12 percent), the capacitor matching among devices was very good (0.69-percent mismatch). The yield was 95 percent.

V. Conclusions

A successful design and implementation of a high-precision low-power time-to-voltage converter and analog memory has been presented. A CMOS time-integration circuit based on saturation-region current switching performs very well, demonstrating that CMOS is well suited for this type of application. The TVC architecture is also easily expandable to implement the analog memory. Future versions of the chip could easily be expanded to 16 or more channels, limited by the added parasitic capacitance at one critical circuit node. The measured time resolution of the eight-channel TVC is 0.4 ns, which allows a 6-bit analog-to-digital conversion.

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References

[1] H. H. Williams, "Design principles of detectors at colliding beams," *Ann. Rev. Nucl. Particle Sci.*, vol. 36, pp. 361–417, 1986.

[2] T. J. Devlin, A. Lankford, and H. H. Williams, "Electronics, triggering, and data acquisition for the SSC," in *Proc. 1986 Summer Study Physics of Superconducting Super Collider* (Snowmass, CO), 1986, pp. 439–454.

[3] B. J. Sheu, D. L. Scharfetter, and P. K. Ko, "SPICE2 implementation of BSIM," Electron. Res. Lab., Univ. of Calif., Berkeley, Memo UCB/ERL M85/42, May 24, 1985.